AMENDMENTS TO THE CLAIMS

This listing of the claims replaces all prior versions, and listings, of claims in the application:

LISTING OF CLAIMS

1. (Cancelled)
2. (Cancelled)
3. (Cancelled)
4. (Cancelled)
5. (Cancelled)
6. (Cancelled)
7. (Cancelled)
8. (Cancelled)
9. (Cancelled)
10. (Cancelled)
11. (Cancelled)
12. (Cancelled)
13. (Cancelled)
14. (Cancelled)
15. (Cancelled)
16. (Cancelled)
17. (Cancelled)
18. (Cancelled)
19. (Cancelled)
20. (Cancelled)
21. (Cancelled)
22. (Cancelled)
23. (Cancelled)
24. (Cancelled)
25. (Cancelled)
26. (Cancelled)
27. (Cancelled)
28. (Cancelled)
29. (Cancelled)
30. (Cancelled)
31. (Cancelled)
32. (Cancelled)
33. (Cancelled)
34. (Cancelled)

35. (Cancelled)

36. **(Original)** A system for extracting design and layout information from a plurality of image-mosaics representative of a deconstructed integrated circuit, the system comprising means for enabling parallel design analysis of the image-mosaics by a plurality of engineer analysts concurrently reverse engineering an IC.

37. **(Original)** A system as claimed in claim 36, wherein the plurality of image-mosaics are annotated concurrently using a plurality of design analysis workstations.

38. **(Original)** A system as claimed in claim 37, wherein each one of the annotation objects created using a design analysis workstation participating in parallel design analysis includes an ownership attribute specifying an engineer analyst associated with the design analysis workstation at a time when the annotation object was created.

39. **(Original)** system as claimed in claim 38, wherein annotation objects include an identification string, and the system further comprises means for generating unique identification strings.

40. **(Original)** A system as claimed in claim 38, wherein annotation objects having different ownership attributes can be merged for display on one design analysis workstation.

41. (Cancelled)

42. (Cancelled)
43. (Cancelled)
44. (Cancelled)
45. (Cancelled)
46. (Cancelled)
47. (Cancelled)
48. (Cancelled)
49. (Cancelled)
50. (Cancelled)
51. (Cancelled)
52. (Cancelled)
53. (Cancelled)
54. (Cancelled)
55. (Cancelled)
56. (Cancelled)
57. (Cancelled)
58. (Cancelled)
59. (Cancelled)
60. (Cancelled)
61. (Cancelled)
62. (Cancelled)
63. (Cancelled)
64. (Cancelled)
65. (Cancelled)
66. (Cancelled)
67. (Cancelled)
68. (Cancelled)
69. (Cancelled)
70. (Cancelled)
71. (Cancelled)

72. **(Original)** A method of analyzing a design of a deconstructed integrated circuit using a design analysis workstation, comprising a step of propagating signal information from an annotation object having a signal property to at least one connected annotation object.

73. **(Original)** A method as claimed in claim 72 further comprising a step of propagating signal information between a cell and a wire annotation object.

74. **(Original)** A method as claimed in claim 73 further comprising a step of generating a net-list from interconnected cells.

75. **(Original)** A method as claimed in claim 72, wherein propagating signal information further comprises steps of:

a) selecting all contact annotation objects connected to a wire annotation object, the wire annotation object and the contact annotation objects having at least one specified layer in common; and

b) propagating signal information from the wire annotation object to all annotation objects connected to the contact annotation objects.

76. **(Original)** A method as claimed in claim 75 further comprising a step of detecting a logical short if two different signals are propagated to a given annotation object.

77. **(Original)** A method as claimed in claim 76, wherein on detecting the logical short the method further comprises a step of displaying information about the logical short on the design analysis workstation.